

## 8-bit shift register with input flip-flops

## 74HC/HCT597

## FEATURES

- 8-bit parallel storage register inputs
- Shift register has direct overriding load and clear
- Output capability: standard
- I<sub>CC</sub> category: MSI

## GENERAL DESCRIPTION

The 74HC/HCT597 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT597 consist each of an 8-bit storage register feeding a parallel-in, serial-out 8-bit shift register. Both the storage register and the shift register have positive edge-triggered clocks. The shift register also has direct load (from storage) and clear inputs.

## QUICK REFERENCE DATA

GND = 0 V; T<sub>amb</sub> = 25 °C; t<sub>r</sub> = t<sub>f</sub> = 6 ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay SH <sub>CP</sub> to Q	C <sub>L</sub> = 15 pF; V <sub>CC</sub> = 5 V	17	20	ns
	ST <sub>CP</sub> to Q		25	29	ns
	$\overline{\text{PL}}$ to Q		21	26	ns
f <sub>max</sub>	maximum clock frequency SH <sub>CP</sub>		96	83	MHz
C <sub>I</sub>	input capacitance		3.5	3.5	pF
C <sub>PD</sub>	power dissipation capacitance per package	notes 1 and 2	29	32	pF

## Notes

1. C<sub>PD</sub> is used to determine the dynamic power dissipation (P<sub>D</sub> in μW):  

$$P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o)$$
 where:  
 f<sub>i</sub> = input frequency in MHz  
 f<sub>o</sub> = output frequency in MHz  
 $\sum (C_L \times V_{CC}^2 \times f_o)$  = sum of outputs  
 C<sub>L</sub> = output load capacitance in pF  
 V<sub>CC</sub> = supply voltage in V
2. For HC the condition is V<sub>I</sub> = GND to V<sub>CC</sub>  
 For HCT the condition is V<sub>I</sub> = GND to V<sub>CC</sub> – 1.5 V

## ORDERING INFORMATION

See "74HC/HCT/HCU/HCMOS Logic Package Information".

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**DC CHARACTERISTICS FOR 74HC**

For the DC characteristics see *"74HC/HCT/HCU/HCMOS Logic Family Specifications"*.

Output capability: standard

I<sub>CC</sub> category: MSI

**AC CHARACTERISTICS FOR 74HC**

GND = 0 V; t<sub>r</sub> = t<sub>f</sub> = 6 ns; C<sub>L</sub> = 50 pF

SYMBOL	PARAMETER	T <sub>amb</sub> (°C)						UNIT	TEST CONDITIONS		
		74HC							V <sub>CC</sub> (V)	WAVEFORMS	
		+25			-40 to +85		-40 to +125				
		min.	typ.	max.	min.	max.	min.				max.
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay SH <sub>CP</sub> to Q		55 20 16	175 35 30		220 44 37		265 53 45	ns	2.0 4.5 6.0	Fig.7
t <sub>PHL</sub>	propagation delay MR to Q		58 21 17	175 35 30		220 44 37		265 53 45	ns	2.0 4.5 6.0	Fig.8
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay ST <sub>CP</sub> to Q		80 29 23	250 50 43		315 63 54		375 75 64	ns	2.0 4.5 6.0	Fig.7
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay PL to Q		69 25 20	215 43 37		270 54 46		325 65 55	ns	2.0 4.5 6.0	Fig.9
t <sub>THL</sub> / t <sub>TLH</sub>	output transition time		19 7 6	75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Fig.9
t <sub>w</sub>	ST <sub>CP</sub> pulse width HIGH or LOW	80 16 14	11 4 3		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig.7
t <sub>w</sub>	SH <sub>CP</sub> pulse width HIGH or LOW	80 16 14	14 5 4		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig.7
t <sub>w</sub>	MR pulse width LOW	80 16 14	22 8 6		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig.8
t <sub>w</sub>	PL pulse width LOW	80 16 14	22 8 6		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig.9
t <sub>rem</sub>	removal time MR to SH <sub>CP</sub>	60 12 10	-3 -1 -1		75 15 13		90 18 15		ns	2.0 4.5 6.0	Fig.10
t <sub>su</sub>	set-up time D <sub>n</sub> to ST <sub>CP</sub>	60 12 10	8 3 2		75 15 13		90 18 15		ns	2.0 4.5 6.0	Fig.11

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		+25			-40 to +85		-40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t <sub>su</sub>	set-up time D <sub>S</sub> to SH <sub>CP</sub>	60 12 10	11 4 3		75 15 13		90 18 15		ns	2.0 4.5 6.0	Fig.11
t <sub>su</sub>	set-up time $\overline{PL}$ to SH <sub>CP</sub>	60 12 10	11 4 3		75 15 13		90 18 15		ns	2.0 4.5 6.0	Fig.12
t <sub>h</sub>	hold time D <sub>n</sub> to ST <sub>CP</sub>	5 5 5	-3 -1 -1		5 5 5		5 5 5		ns	2.0 4.5 6.0	Fig.11
t <sub>h</sub>	hold time $\overline{PL}$ , D <sub>S</sub> to SH <sub>CP</sub>	5 5 5	-6 -2 -2		5 5 5		5 5 5		ns	2.0 4.5 6.0	Fig.11
f <sub>max</sub>	maximum pulse frequency SH <sub>CP</sub>	6.0 30 35	29 87 104		4.8 24 28		4.0 20 24		MHz	2.0 4.5 6.0	Fig.7